LAB 5: Serial Adder and Shift Registers

Objectives
In your last lab you should have successfully designed and simulated a 4-bit parallel adder that is commonly referred to as a ripple adder. In this lab you will build and test a serial adder, a parallel to serial shift register and a serial to parallel shift register.

Materials
Prototyping bread board, switches, Resistors, LEDs, Wires, CPLD Breakout Board

Pre-Lab Part I. Serial Adder
1. Design a serial adder, using a full adder and a D flip-flop, as shown in Figure 1 in the appendix. Draw it in Quartus and simulate the serial addition for the following numbers shown below. Reset your serial adder after every addition. Why is this necessary to do this?
   - A= 1010, B = 0101
   - A= 1111, B = 0001
   - A= 1100, B= 1001
   - A= 1101, B= 1011

2. Print and bring the circuit schematics, simulation results, and your Quartus II simulation files to lab. Also email your design & simulation files as was done in previous labs.

Pre-Lab Part II. Parallel to Serial Conversion
1. Design a 4-bit parallel to serial shifter using (4) D Flip-Flops and (4) 2:1 Muxes in Quartus. The component should have 4 inputs (D3:0), a clock (CLK), a load/shift input signal (+LD/+SHF) and one serial output (Y). Additional design details will be covered in class.

2. Test (simulate) your design in Quartus by clocking in the following parallel nibbles below and then clocks the bits out one at a time until all bits have been observed at the output Y.
   - D3:0 = 5
   - D3:0 = A
   - D3:0 = 9
   - D3:0 = 6

3. Print and bring the circuit schematics, simulation results, and your Quartus II simulation files to lab. Also email your design & simulation files as was done in previous labs.

Note: All pre-lab material must be turned in at the start of lab.

In-Lab Part I & II
Download to your design to your CPLD and demonstrate functionality with switches (data, clock, reset) for inputs and LEDs for output to your TA. It is highly advised that you have this ready & functional before entering lab.

In-Lab Part III
Download your serial adder and serial to parallel converter to your CPLD. Connect switches for inputs and LEDs for outputs.

Note: The clock input to the D flip-flop (CLK) should be generated by a switch de-bouncing circuit. See Figure 2 for further details.

Your TA will now give you two values to add serially and then observe the correct result as a parallel value on your outputs. You must be able to explain how the inputs are clocked in and what the expected output should be as it passes through the serial to parallel converter.

In-Lab Quiz
During the first or last half hour of lab, your TA will give you an input waveform for either the serial adder, parallel to serial converter or serial adder/serial to parallel converter circuitry. You task will be to accurately draw the output waveform based on the input signal and a clock.

simulation files to lab. Also email your design & simulation files as was done in previous labs.
Point Break-down

Pre-Lab Part I Materials 10%
Pre-Lab Part II Materials 10%
Pre-Lab Part III Materials 10%
In-Lab Quiz 25%

Figure 1. Serial Adder.

Figure 2. Switch De-bounce Circuit for Clock Generation

Single pole, double throw (SPDT) switch

CLK (to be used as the clock input of the D flip-flop in the above serial adder circuit.)