LAB 3: Multiplexers and Decoders

Objectives
The objective of this lab is to familiarize students with the design, operation, and application of multiplexers and decoders.

Materials
• Prototyping board
• Wires
• IC's: Any gates available in your lab kit. i.e. AND, OR, NAND, NOR, Inverters, etc.

Part I. Multiplexer/Pre - Lab
The multiplexer (MUX) is a device that acts as a multi-position switch. See Figure 1. A number of DATA inputs are applied to this device (D0-D3) and one of the inputs is switched to the output (Y) of the device. A binary number applied to the SELECT (S1 & S0) lines controls which input is passed to the output. For example, when S1=S0=0, D0 is connected to the output Y. When S1=0 & S0=1, D1 connects to Y and so forth for D2 & D3 to connect to Y. Note that for the MUX shown in Figure 1, S1:0 are active low and all other signals are active high.

1. Draw a logic table for the 4:1 Multiplexer shown in Figure 1, using “don't cares” as appropriate.
2. Write the logic equation for this MUX.
3. Draw a voltage table for this MUX.
4. Design a circuit for this MUX (by hand) using logic gates available in the ICs listed above in the “Materials” section above.
5. Draw and simulate the complete mixed-logic circuit in Quartus II. Add pin numbers and chip labels to the circuit diagram to make this a wiring diagram.

Turn in the printouts of the logic table, logic equation, voltage table, Quartus circuit schematic and simulation results. Also email the Quartus design file to your TA. All pre-lab materials are to be turned in at the beginning of lab. Therefore, please make copies of all material you will need in-lab to complete demonstration of a working circuit.

Part I. Multiplexer/In-Lab
Build your Pre-Lab’s MUX solution and test it at home. Demonstrate its function to your TA in lab. You can demonstrate your circuit’s operation by connecting appropriate switch circuits to all inputs and an appropriate LED circuit to the output. Go through the different switch combinations with the TA to verify full functionality.

Part II. Decoder/Pre-Lab
A decoder starts with a binary number (pattern) and then decodes it to an individual output signal. For example, in the 2:4 Decoder shown in Figure 2, a two bit binary number (A1:0) is decoded such that only one of the 4 active low outputs are enabled. For example, when A1=A0=0, only Y0 goes true; when A1=0 and A0=1, only Y1 goes true and so forth for the remaining two A1 and A0 combinations.

Additional Notes: The 2:4 Decoder below has a active low global enable. This functions in the following manner. When the enable is false (high), all outputs are false. When the enable is true (low), an output will go true based on the binary pattern placed on A1:0 (as described above).
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1. Draw **logic tables** for the decoder in Figure 2.
2. Create **logic equations** for each of the outputs.
3. Draw **voltage tables** for the above decoder.
4. Design a **circuit** (by hand) to implement the design.
5. **Draw** and **simulate** the complete mixed-logic circuits in Quartus. Add pin numbers and chip labels to the circuit diagram to make this a wiring diagram.

Turn in all the above pre-lab materials in printed form and email the Quartus design file to your TA. Be able to answer questions on your design.

**Part II. Decoder/In-Lab**
Build your 2:4 decoder (at home) and demonstrate its function to your TA in lab. Use appropriate switch circuits for the inputs and LED circuits for the outputs.

**Part III. In-Lab Quiz**
The TA will ask you to design a component similar to the one in Figure 1 or Figure 2. You are to provide for it a **logic table**, **logic equation**, a **voltage table** and a **circuit** diagram. **Then, you are to enter the design into Quartus, simulate, build and demonstrate it to your TA.**

**Final Notes**
You should wire Pre-Lab Parts I & II at home before attending lab. Otherwise, you will not have enough time to finish lab. All inputs must come from switches and all outputs must go to LEDs.

Upon leaving lab, all breadboard circuits must be removed from your breadboard such that the breadboard is completely blank. Also email all your Quartus schematic entry files to your TA. The subject line MUST include the lab number, section number and your name in the following order: Lab1 2960 Jose Cuervo. You name must also be inside the design file. Failure to do this will result in a 50% penalty being assessed to your Lab #3 point total.

**Point Break Down**
Pre-lab Part I. Logic Truth Table, Logic Equation, Voltage Table, Schematic & Simulation results. 10%
In-lab Part I. bread-boarded circuit functional demonstration. 10%

Pre-lab Part II. Logic Truth Table, Logic Equation, Voltage Table, Schematic & Simulation results. 10%
In-lab Part II. Bread-boarded circuit functional demonstration. 10%

In-lab Part III Quiz. Logic Equation, Voltage Table, paper circuit design. 15%
In-lab Part III Quiz. Quartus circuit design & simulation. 15%
In-lab Part III Quiz. Breadboard circuit construction & functional demonstration. 30%