Conversion of one type of flip-flop to another is usually possible by adding external gates. Figure 11-24 shows how a J-K flip-flop and a D flip-flop can be converted to a T flip-flop.

Problems

11.1 Assume that the inverter in the given circuit has a propagation delay of 5 ns and the AND gate has a propagation delay of 10 ns. Draw a timing diagram for the circuit showing X, Y, and Z. Assume that X is initially 0, Y is initially 1, after 10 ns X becomes 1 for 80 ns, and then X is 0 again.

11.2 A latch can be constructed from an OR gate, an AND gate, and an inverter connected as follows:

(a) What restriction must be placed on R and H so that P' will always equal \( Q' \) (under steady-state conditions)?
(b) Construct a next-state table and derive the characteristic (next-state) equation for the latch.
(c) Complete the following timing diagram for the latch.

11.3 This problem illustrates the improper operation that can occur if both inputs to an S-R latch are 1 and are then changed back to 0. For Figure 11-6, complete the following timing chart, assuming that each gate has a propagation delay of exactly 10 ns. Assume that initially \( P = 1 \) and \( Q = 0 \). Note that when \( t = 100 \) ns, S and R are both changed to 0. Then, 10 ns
later, both \( P \) and \( Q \) will change to 1. Because these 1's are fed back to the gate inputs, what will happen after another 10 ns?

11.4 Design a gated D latch using only NAND gates and one inverter.

11.5 What change must be made to Figure 11-15(a) to implement a falling-edge triggered D flip-flop? Complete the following timing diagram for the modified flip-flop.

11.6 A reset-dominant flip-flop behaves like an S-R flip-flop, except that the input \( S = R = 1 \) is allowed, and the flip-flop is reset when \( S = R = 1 \).
(a) Derive the characteristic equation for a reset-dominant flip-flop.
(b) Show how a reset-dominant flip-flop can be constructed by adding gate(s) to an S-R flip-flop.

11.7 Complete the following timing diagram for the flip-flop of Figure 11-20(a).
11.8 Complete the following diagrams for the falling-edge triggered D-CE flip-flop of Figure 11-27(c). Assume $Q$ begins at 1.
(a) First draw $Q$ based on your understanding of the behavior of a D flip-flop with clock enable.

(b) Now draw in the internal signal $D$ from Figure 11-27(c), and confirm that this gives the same $Q$ as in (a).

11.9 (a) Complete the following timing diagram for a J-K flip-flop with a falling-edge trigger and asynchronous ClrN and PreN inputs.

(b) Complete the timing diagram for the following circuit. Note that the Ck inputs on the two flip-flops are different.
11.10 Convert by adding external gates:
(a) a D flip-flop to a J-K flip-flop.
(b) a T flip-flop to a D flip-flop.
(c) a T flip-flop to a D flip-flop with clock enable.

11.11 Complete the following timing diagram for an S-R latch. Assume \( Q \) begins at 1.

11.12 Using a truth table similar to Table 11-1, confirm that each of these circuits is an S-R latch. What happens when \( S = R = 1 \) for each circuit?

11.13 Complete the following timing diagrams for a gated D latch. Assume \( Q \) begins at 0.
(a) First draw \( Q \) based on your understanding of the behavior of a gated D latch.

(b) Now draw in the internal signals \( S \) and \( R \) from Figure 11-11, and confirm that \( S \) and \( R \) give the same value for \( Q \) as in (a).
11.14 Complete the following diagrams for the rising-edge triggered D flip-flop of Figure 11.15. Assume $Q$ begins at 1.
(a) First draw $Q$ based on your understanding of the behavior of a D flip-flop.

![Diagram of rising-edge triggered D flip-flop]

(b) Now draw the internal signal $P$ from Figure 11.15, and confirm that $P$ gives the same $Q$ as in (a).

11.15 A set-dominant flip-flop is similar to the reset-dominant flip-flop of Problem 11.6 except that the input combination $S = R = 1$ sets the flip-flop. Repeat Problem 11.6 for a set-dominant flip-flop.

11.16 Fill in the timing diagram below for a falling-edge triggered S-R flip-flop. Assume $Q$ begins at 0.

![Timing diagram of falling-edge triggered S-R flip-flop]

11.17 Fill in the timing diagram below for a falling-edge triggered J-K flip-flop.
(a) Assume $Q$ begins at 0.

![Timing diagram of falling-edge triggered J-K flip-flop]

(b) Assume $Q$ begins at 1, but Clock, $J$, and $K$ are the same.
11.18 (a) Find the input for a rising-edge triggered D flip-flop which would produce the output $Q$ as shown. Fill in the timing diagram.
(b) Repeat for a rising-edge triggered T flip-flop.

11.19 Here is the diagram of a 3-bit ripple counter. Assume $Q_0 = Q_1 = Q_2 = 0$ at $t = 0$, and assume each flip-flop has a delay of 1 ns from the clock input to the $Q$ output. Fill in $Q_0$, $Q_1$, and $Q_2$ of the timing diagram. Flip-flop $Q_1$, will be triggered when $Q_0$ changes from 0 to 1.

11.20 Fill in the following timing diagram for a rising-edge triggered T flip-flop with an asynchronous active-low PreN input. Assume $Q$ begins at 1.
11.21 The ClrN and PreN inputs introduced in Section 11.8 are called asynchronous because they operate independently of the clock (i.e., they are not synchronized with the clock). We can also make flip-flops with synchronous clears or preset inputs. A D-flip-flop with an active-low synchronous ClrN input may be constructed from a regular D flip-flop as follows.

\[
\begin{array}{c}
D \\
\text{ClrN} \\
\text{Clnk}
\end{array}
\quad
\begin{array}{c}
D \\
Q
\end{array}
\]

Fill in the timing diagram. For \( Q_{11} \), assume a synchronous ClrN as above, and for \( Q_{12} \), assume an asynchronous ClrN as in Section 11.8. Assume \( Q_1 = Q_2 = 0 \) at the beginning.

\[
\begin{array}{c|c|c|c|c|c|c|c|c|c|c|c|c|}
\text{Clock} & & & & & & & & & & & & \\
\text{ClrN} & & & & & & & & & & & & \\
D & & & & & & & & & & & & \\
Q_1 & & & & & & & & & & & & \\
Q_2 & & & & & & & & & & & & \\
\end{array}
\]

11.22 (a) Construct a D flip-flop using an inverter and an S-R flip-flop.
(b) If the propagation delay and setup time of the S-R flip-flop in (a) are 2.5 ns and 1.5 ns, respectively, and if the inverter has a propagation delay of 1 ns, what are the propagation delay and setup time of the D flip-flop of part (a)?

11.23 Redesign the debouncing circuit of Figure 11-9 using the \( \overline{S-R} \) latch of Figure 11-10.

**Programmed Exercise 11.24**

Cover the bottom part of each page with a sheet of paper and slide it down as you check your answers.

The internal logic diagram of a falling-edge triggered D flip-flop follows. This flip-flop consists of two basic S-R latches with added gates. When the clock input (\( \text{CK} \)) is 1, the value of \( D \) is stored in the first S-R latch (\( P \)). When the clock changes from 1 to 0, the value of \( P \) is transferred to the output latch (\( Q \)). Thus, the operation is similar to that of the master-slave S-R flip-flop shown in Figure 11-19, except for the edges at which the data is stored.