Open book and open notes, 90-minute examination to be done in non-red pencil or pen.

- No electronic devices permitted. All work and solutions are to be written on the exam where appropriate.
- CHECK YOUR ANSWERS Twice/Three Times - Regrades will only be for pts. added up incorrectly!

**Point System:**

<table>
<thead>
<tr>
<th>Pages</th>
<th>Points</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/2</td>
<td>19</td>
</tr>
<tr>
<td>3</td>
<td>17</td>
</tr>
<tr>
<td>4</td>
<td>14</td>
</tr>
<tr>
<td>TOTAL</td>
<td></td>
</tr>
</tbody>
</table>

(50 pt.)

Grade Review Information: (NOTE: deadline of request for grade review is the day the exam is returned.)

---

1. Using only 2 input NOR gates, implement the following logic equation (do not simplify).

   Your final answer should only contain 2 input NOR Gates Only!  (4 pt);

   \[ Y = \overline{A \cdot B}(C+\overline{D}) \]

   ; Y.H, A.L, B.H, C.L, D.L
2. Assume that a vector of 8 bit 2's complement numbers are stored in memory starting at 2000 Hex. The number of elements in the vector is less than 256 and the last element is set to zero to denote the end of vector. Note: Other than the end of vector element, no other elements are zero.

Write a G-CPU program to count the number of negative numbers in the vector and place this sum at memory location 4000 Hex. You may assume that the value at 4000 Hex is initially zero. (9 pt.)

Write your answer in the leftmost column lines. If you need more room, wrap around to the right column lines.

3. Refer to the attached G-CPU program on the last page of this quiz. Assume the code was placed in ROM starting at $8000. Also assume there is RAM starting at $9000. Answer the questions below:

3A. What are the byte values in ROM memory for addresses $8000 to $8009? (5 pt.)

8000 [ ____________ ]  8001 [ ____________ ]  8002 [ ____________ ]  8003 [ ____________ ]
8004 [ ____________ ]  8005 [ ____________ ]  8006 [ ____________ ]  8007 [ ____________ ]
8008 [ ____________ ]  8009 [ ____________ ]

3B. If the clock is 10 MHz, how many seconds does it take to execute the first LDX #$9000 instruction? (1 pt.)
3C. What does this program perform? The most precise answer will receive the most points. (2 pt.)

3D. Fill out the cycle diagram below for the second time the following two lines are executed in the program given in Appendix A. (8 pt.)

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Addr Bus</th>
<th>Data Bus</th>
<th>IR</th>
<th>PC</th>
<th>R/-W</th>
<th>A Reg</th>
<th>Y Reg</th>
<th>Reg Driving Addr Bus</th>
<th>Device Driving Data Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

;this instruction starts at address $8015 in ROM memory

4. We would like to add three new branch instructions to the G-CPU. These are

BRA Addr ;unconditional branch, always branch
BC Addr  ;branch if there is a carry after a sum operation
BNC Addr ;branch if there is no carry after a sum operation

4A. What new hardware or signals must be added to the G-CPU to create these three new instructions? (2 pt.)

4B. Show what must be added to the G-CPU Controller ASM below for these three new instructions. (5 pt.)
5. For the following problem, assume that you have the hardware you used in Lab #9 and the ASM Controller flow chart on the next page. Fill in the timing diagram below assume that the first six nibbles in ROM memory are 1, A, 4, 0, 7, B. i.e. ROM Contents: Addr0 [1], Addr1 [A], Addr2 [4], Addr3 [0], Addr4 [7], Addr5 [B]. (10 pt.)

![Timing Diagram](image)

Fill in all the blank area above!  *A3:0 = Register A3:0 in the ALU

6. We would like to create a new instruction for the G-CPU called STX addr which stores the contents of X into memory starting at the address specified by the operand addr. Show the required hardware modification to the X Block (2 pt.) below and the changes required to the C-CPU ASM Controller Flow Chart (2 pt.)

Hardware Modifications:  ASM Flow Chart Modifications:
G-CPU Code for Problem #3:

```
ORG $8000
LDX #$9000     ;ptr to input data
LDY #$9800     ;ptr to counter and result
LDAA #$24      ;initial counter value
STAA 0,Y
LDAA #0
STAA 1,Y

T1	       LDAA 0,X
           INX
           BNE SKIP1
           LDAA 1,Y
           LDAB #1
           SUM_BA
           STAA 1,Y

SKIP1	     LDAB #$FF
           LDAA 0,Y
           SUM_BA
           STAA 0,Y
           BNE T1

END1	      BEQ END1
```

ASM Controller Flow Chart for Problem #5: