1. A student has purchased a microprocessor that has a 20 bit address bus and 16 bit data bus. How many maximum bits, bytes and words can this microprocessor address? Show your values as a power of 2. i.e. $2^{20}$ (3 pt.)

$$\text{words} = \frac{2^{20}}{8}, \quad \text{bytes} = \frac{2^{21}}{8}, \quad \text{bits} = \frac{2^{24}}{8}$$

2. Given the input and output current characteristics for an Altera 3064 CPLD in Appendix A, what is the worst case estimate for the number of input pins that can be driven by one output pin? Show all equations below and do not solve with a calculator; just show as fractions and state how to find the worst case. (4 pt.)

$$\frac{-27mA}{200mA}$$

$$\frac{35mA}{245mA}$$

pick smallest integer
3. You are given a microprocessor with a **16 bit address bus** and **8 bit data bus**. The control bus consists of a R/W signal and a low true data strobe (-DS). Upon reset, the processor begins fetching the first instruction address from the **highest two addresses in the memory map**. You are given any number of **4K x 8 ROMs** and **8K x 4 SRAMs**. Place **5K of ROM** in the system and **16K of SRAM** starting at **4000 Hex** in the system memory map. Show the required Rom & Ram memory devices below. Label all signals and use bus nomenclature where appropriate. Note: The decode equations will go on the next page. (16 pt.)
4. For the previous problem show the required decode circuitry for the ROM devices below. Your decode signals you are going to create below should match those that you specified on the previous page. (8 pt.)

$\text{Highest} \ 4K - \text{Rom } 0 = A_{15}, A_{14}, A_{13}, A_{12}, -DS, R/W$

$50 - \text{Rom } 1 = A_{15}, A_{14}, A_{13}, \overline{A_{12}}, A_{11}, A_{10}, -DS, R/W$

5. What is the address range of the ROM block? (2 pt.)

$EC00 - FFFF$

6. Show the decode circuitry for the RAM devices you drew on the previous page. Your decode signals that you are going to create below should match those that you specified on the previous page. (6 pt.)

$3 - \text{Ram } 0 = \overline{A_{15}}, A_{14}, A_{13}, -DS$

$3 - \text{Ram } 1 = \overline{A_{15}}, A_{14}, A_{13}, -DS$

7. What would the decode logic equations be for the RAM block if the starting address for the RAM is 3000 Hex? (4 pt.)

$0011 \ 3000 - 3FFF 4K 2 - \text{Ram } 0 = (\overline{A_{15}}, A_{14}, A_{13}, A_{12}, + \overline{A_{15}}, A_{14}, A_{13}, A_{12}) \cdot -DS$

$0100 \ 4000 - 4FFF 4K$

$0101 \ 5000 - 5FFF 4K$

$0110 \ 6000 - 6FFF 4K 2 - \text{Ram } 1 = (\overline{A_{15}}, A_{14}, A_{13}, A_{12}, + \overline{A_{15}}, A_{14}, A_{13}, A_{12}) \cdot -DS$

8. What values should be programmed into the highest two bytes of the ROM placed in the highest address range? (2 pt)

$EC, 00$
9. Use the ASM Diagram in Appendix B. to complete the following problems. Assume that JK flip-flops will be used for the state variables and that the output of the most significant flip-flop is Q1 and the output of the least significant flip-flop is Q0. Fill out the next state LOGIC table for the design below. (14 pt.)

<table>
<thead>
<tr>
<th>A.L</th>
<th>Q1.H</th>
<th>Q0.H</th>
<th>Q1.H+</th>
<th>Q0.H+</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>DO</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>X</td>
<td>1</td>
<td>X</td>
<td>0</td>
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<tr>
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<td>0</td>
<td>X</td>
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<td>x</td>
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<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
</tbody>
</table>

10. Assuming that we will use logic devices (AND, OR & Inverter gates) to implement the design. Show the simplified logic equations required for J1, K0 and X. (7 pt.)

\[
J1 = \overline{A} \overline{Q_0}
\]

\[
K0 = 1 \text{ or } \overline{Q_0}
\]

\[
X = A + Q1
\]

- 1 for \( \overline{Q_0} \overline{Q_1} \overline{A} \overline{P_1} \)
- 3 if had K's for state 3

Page 4
11. For the next state logic table in problem #9 (ASM Diagram in Appendix B.), assume that the design will now be implemented in an 32K x 8 EPROM and that all unused address lines are tied high. Draw the EPROM connections below and show what must be programmed in the EPROM. Don't care data should programmed as zeros for ease of grading purposes. (14 pt.)

EPROM Circuit Below

EPROM Memory Address & Contents

<table>
<thead>
<tr>
<th>Address (Hex)</th>
<th>Data (Hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7FF8 2</td>
<td>02 LLL LHL</td>
</tr>
<tr>
<td>7FF 9</td>
<td>08 LLL HLL</td>
</tr>
<tr>
<td>7FF A</td>
<td>23 LHL LHH</td>
</tr>
<tr>
<td>7FF 8</td>
<td>80 LLL LLL</td>
</tr>
<tr>
<td>7FF C</td>
<td>16 LCH LHL</td>
</tr>
<tr>
<td>7FF D</td>
<td>40 HLL LHL</td>
</tr>
<tr>
<td>7FF E</td>
<td>23 LHL LHH</td>
</tr>
<tr>
<td>7FF F</td>
<td>00 LLL LLL</td>
</tr>
</tbody>
</table>

12. For the specifications given for the Fish Tank Controller in Appendix C, draw the required flow chart below. (8 pt.)

3 states + 1
Pump + 1
Heat + 2
UV light 2
Bubbler 2
14. Using the design found in Appendix D, complete the voltage timing diagram below.

Note1: You do not have to draw propagation delays in the diagram below. However you should take them into account when deriving the sum and flip-flop outputs in each clock cycle.

Note2: -reset is asynchronous and functions just as was observed in your CPLD; WXYZ are all unknown initially at time zero. (12 pt.)

Complete the Voltage Timing Diagram Below