Open book/open notes, 90-minutes. Calculators are permitted. Write on the top of each page only.

Page 1) 7 points ______________
Page 2) 16 points ______________
Page 3) 22 points ______________
Page 4) 21 points ______________
Page 5) 22 points ______________
Page 6) 12 points ______________
TOTAL ______________ out of 100

Grade Review Information: 1. Deadline of request for grade review is the day the exam is returned. 2. Do not make any changes to problems in the test as this will be considered cheating. 3. Write only in this blocked area for a re-grade request. 4. Simply write the problem number that you would like re-graded. 3 Maximum.

_______________________________________________________________________________
________________________________________________________________________________________
________________________________________________________________________________________
________________________________________________________________________________________
________________________________________________________________________________________
________________________________________________________________________________________
________________________________________________________________________________________
________________________________________________________________________________________

1. A student has purchased a microprocessor that has a 20 bit address bus and 16 bit data bus. How many maximum bits, bytes and words can this microprocessor address? Show your values as a power of 2. i.e. 2^8 (3 pt.)

words = ____________________ bytes = ____________________ bits = ____________________

2. Given the input and output current characteristics for an Altera 3064 CPLD in Appendix A, what is the worst case estimate for the number of input pins that can be driven by one output pin? Show all equations below and do not solve with a calculator; just show as fractions and state how to find the worst case. (4 pt.)
3. You are given a microprocessor with a **16 bit address bus** and **8 bit data bus**. The control bus consists of a **R/W** signal and a low true data strobe (**-DS**). Upon reset, the processor begins fetching the first instruction address from the **highest two addresses in the system memory map**. You are given any number of **4K x 8 ROMs** and **8K x 4 SRAMs**. Place **5K of ROM** in the system and **16K of SRAM** starting at **4000 Hex** in the system memory map. Show the required Rom & Ram memory devices below. Label all signals and use bus nomenclature where appropriate. Note: The decode equations will go on the next page. (16 pt.)
4. For the previous problem show the required decode circuitry for the ROM devices below. Your decode signals you are going to create below should match those that you specified on the previous page. (8 pt.)

5. What is the address range of the ROM block? (2 pt.)

6. Show the decode circuitry for the RAM devices you drew on the previous page. Your decode signals that you are going to create below should match those that you specified on the previous page. (6 pt.)

7. What would the decode logic equations be for the RAM block if the starting address for the RAM is 3000 Hex? (4 pt.)

8. What values should be programmed into the highest two bytes of the ROM to accommodate the reset vector mentioned in #3? (2 pt.)
9. Use the ASM Diagram in Appendix B. to complete the following problems. Assume that JK **flip-flops** will be used for the state variables and that the **output of the most significant flip-flop is** \( Q_1 \) and the **output of the least significant flip-flop is** \( Q_0 \). Fill out the **next state LOGIC table** for the design below. (14 pt.)

\[
\begin{array}{cccccccccccc}
\end{array}
\]

10. Assuming that we will use logic devices (AND, OR & Inverter gates) to implement the design. Show the **simplified logic equations** required for \( J1 \), \( K0 \) and \( X \). (7 pt.)

\[
\begin{align*}
J1 &= \quad \quad \quad \quad \quad \quad \\
K0 &= \quad \quad \quad \quad \quad \quad \\
X &= \quad \quad \quad \quad \quad \quad \\
\end{align*}
\]
11. For the next state logic table in problem #9 (ASM Diagram in Appendix B.), assume that the design will now be implemented in an 32K x 8 EPROM and that all unused address lines are tied high. Draw the EPROM connections below and show what must be programmed in the EPROM. Don’t care data should programmed as zeros for ease of grading purposes.  

<table>
<thead>
<tr>
<th>EPROM Memory Address &amp; Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address (Hex)</td>
</tr>
<tr>
<td>Data (Hex)</td>
</tr>
</tbody>
</table>

12. For the specifications given for the Fish Tank Controller in Appendix C, draw the required flow chart below. (8 pt.)
14. Using the design found in Appendix D, complete the **voltage timing diagram** below.

Note1: You do not have to draw propagation delays in the diagram below. However you should take them into account when deriving the sum and flip-flop outputs in each clock cycle.

Note2: -reset is asynchronous and functions just as was observed in your CPLD; WXYZ are all unknown initially at time zero. (12 pt.)

---

**Complete the Voltage Timing Diagram Below**

-reset

CLK

N1

H

L

N2

H

L

SUM

H

L

Cout

H

L

Cin

H

L

W

H

L

X

H

L

Y

H

L

Z

H

L
Appendix A. Altera CPLD Input and Output Current Requirements

<table>
<thead>
<tr>
<th></th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{OH}$</td>
<td>-27 mA</td>
<td>-29 mA</td>
<td>-32 mA</td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td>35 mA</td>
<td>39 mA</td>
<td>43 mA</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>160 uA</td>
<td>180 uA</td>
<td>200 uA</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>-220 uA</td>
<td>-230 uA</td>
<td>-245 uA</td>
</tr>
</tbody>
</table>

Appendix B. Typical ASM Diagram

State 0

F  A.L  T

State 1

Y.L

Z.H

F  A.L  T

State 2

X.L

Z.H

J  K  Q+  Q  /Q

0  0  0  Q
0  1  0
1  0  1
1  1  /Q
Appendix C. Fish Tank Controller

We would like to design a flow chart for a fish tank controller. Here are the specifications:

**Outputs:** Heater.H (when on/true heats up the water), Bubbler.L (when on/true, injects bubbles into the water), Pump.L (when on/true, pumps the water through a filter), UV_Light.H (when on/true, turns on bacteria killing UV light)

**Inputs:** TempSensor.L (goes true when the temperature in the tank is below the desired temperature set-point), PhotoSensor.H (goes true when the water is murky due to excessive bacteria & dirt in the water)

1. The period of the clock is one minute.
2. The Pump should always be pumping water through the filter at any time.
3. The Heater should only go on when the water temperature is below the desired set-point.
4. The UV_Light should only go on for a maximum of two minutes if both the temperature is below the setpoint and the PhotoSensor detects murky water. Once the temperature reaches setpoint and the PhotoSensor detects clear water, UV Light should immediately be shut off.
5. The Bubbler should be on for at least one minute for every three minutes of pump operation and the bubbler should be turned on if the PhotoSensor detects murky bad water.

*The optimal flow chart implementing the above rules will be awarded the most points.*

Appendix D. Serial Adder with Parallel Converter