Last Name, First Name

Page 1) 9 points

Page 2) 16 points

Page 3) 16 points

Page 4) 18 points

Page 5) 20 points

Page 6) 12 points

Page 7) 11 points

TOTAL     of 102

Re-grade requests must be handed in the day exams are returned in class. Write the problem number you wish reviewed. A maximum of three problems is allowed for review.

1. Write -45 decimal as a 7 bit signed binary number and then sign extend to 16 bits.

-45 decimal = _______________________________ (signed 7 bits, 2 pt.)

= _______________________________ (signed 16 bits, 1 pt.)

2. Perform the following binary additions and subtractions by hand. Show all your work below. Assume the numbers are all unsigned binary. (2,2,2 pt.)

\[
\begin{align*}
101010 & \quad + \quad 111111 & \quad + \quad 101011 & \quad = \quad 1101.01 \\
11101010 & \quad - \quad 10110111 & \quad \times \quad 10.101 & \\
\end{align*}
\]

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3. Directly synthesize a circuit for the following equation using only 2 Input NAND gates. (8 pt.)

\[ Y = \overline{W \cdot X} + \overline{W + Z} \; ; \; Y, H, W, H, X, L, Z, H \quad \text{Do Not Simplify the Equation!} \]

4. Find the minimum sum of products and minimum product of sums for the logic equation below using a K-Map. (8 pt.)

\[ Y = \overline{A \cdot D} + A \cdot C \cdot \overline{D} + B \cdot C \cdot \overline{D} + \overline{B \cdot C} + A \cdot B \cdot \overline{C} \cdot \overline{D} \]

\[ Y \; \text{(MSOP)} = \]

\[ Y \; \text{(MPOS)} = \]
5. Create a circuit for the following equation using any 1, 2 or 3 input gates. The best solution will receive the maximum points. Use as few gates as possible but do not simplify the equation. (8 pt.)

\[ Y = (X+\overline{W}*Z) + (W*\overline{Z}*V) \]; Y.L, X.H, W.L, Z.H, V.L  Do Not Simplify the Equation!

6. Simplify the equation below with De Morgan’s Rule and Boolean Identities to find a MSOP. (8 pt.)

\[ P = \overline{X} * Y + X + \overline{W} + \overline{Y} * \overline{W} + X*(\overline{W}+\overline{Y}) + \overline{X} * Y \]

\[ Y = \overline{\text{MSOP}} \]
7. Derive the logic equations for the following signals listed after the circuit below. **DO NOT SIMPLIFY.**

\[ \text{P.L} = \ldots \] (2 pt.)

\[ \text{Y.H} = \ldots \] (6 pt.)

8. Design a single bit comparator with one digital output \( Y \). Compare (2) **single bit numbers** such that if inputs \( A = B \) then output \( Y = T \) else \( Y = F \). Assume all inputs and outputs to be low true and your design should be cascade-able. In #9, you will be asked to show how to use this device to compare (2) 3 bit signed numbers so you must created a device that can be cascaded for larger numbers than one bits. Show the logic equation and required circuit below for the \( Y \) output. Also draw the block diagram for the part. (10 pt.)

Block Diagram for the part =>

Logic Equation for \( Y = \)

Circuit for \( Y = \)
9. Using the part you created in #8, show how it can be cascaded to compare (2) 3 bit signed numbers. Label all signals. (4 pt.)

10. Design a device that negates a (4) bit 2's complement number. i.e. -2 => +2, +2 => -2, etc. The part should have four inputs B3:0 and four outputs Y3:0. The part will also require an Error output bit for a particular case that is not possible with this device. Assume all I/O are high true. (16 pt.)

Truth Table =>

Derive the Logic Equations for Y3, Y0 and E in MSOP form =>
11. Show how the part you created in #10 along with any other device of your choice can be used to perform the following computation $D = A - B$ where $A$, $B$ and $D$ are all 4 bit signed numbers. (4 pt.)

12. Implement the logic equation $Y = (A*B + C + D*E + A*B + C + D*E + A*E + B + C + D*E)$ (Y.L, A.H, B.L, C.H, D.H, E.L, F.L) with the following two components. (1) 3:8 decoder with high true select lines, a low true enable and low true outputs. (1) 4:1 mux with high true select lines, high true inputs and outputs. (6 pt.)
14. For the state machine shown below, complete the timing diagram and derive the next state diagram for the state machine. (10 pt.)

Complete the Timing Diagram below for D2, D0, Q2, Q1 and Q0 (9 pt.):

Show the State Diagram for the above design (2 pt.):