1. Perform the following binary addition, subtraction and multiplication by hand. *Show all your work below for full credit.* Assume the numbers are all *unsigned binary.* (3,3,3 pt.)

\[
\begin{align*}
11101.011 + 11111.111 - 10010111 \times 10.001
\end{align*}
\]
2. Given the following logic truth table, simplify with the K-Map below into Minimum Sum of Products (MSOP) and Minimum Product of Sums (MPOS). Assume all signals are low true. (8, 1 pt.)

<table>
<thead>
<tr>
<th>ABCD</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>0</td>
</tr>
<tr>
<td>0001</td>
<td>1</td>
</tr>
<tr>
<td>0010</td>
<td>1</td>
</tr>
<tr>
<td>0011</td>
<td>X</td>
</tr>
<tr>
<td>0100</td>
<td>0</td>
</tr>
<tr>
<td>0101</td>
<td>0</td>
</tr>
<tr>
<td>0110</td>
<td>1</td>
</tr>
<tr>
<td>0111</td>
<td>0</td>
</tr>
<tr>
<td>1000</td>
<td>1</td>
</tr>
<tr>
<td>1001</td>
<td>1</td>
</tr>
<tr>
<td>1010</td>
<td>1</td>
</tr>
<tr>
<td>1011</td>
<td>X</td>
</tr>
<tr>
<td>1100</td>
<td>1</td>
</tr>
<tr>
<td>1101</td>
<td>1</td>
</tr>
<tr>
<td>1110</td>
<td>1</td>
</tr>
<tr>
<td>1111</td>
<td>0</td>
</tr>
</tbody>
</table>

Y (MSOP) = __________________________
Y (MPOS) = __________________________

Is the MSOP Solution equal to the MPOS Solution? ________________________________

3. Simplify the equation below with De Morgan's Rule and Boolean Identities to find a MSOP. (9 pt.)

\[ Y = (\overline{A} + \overline{C}) (\overline{A} \cdot B) (\overline{B} + \overline{C}) (\overline{A} \cdot B \cdot \overline{C}) + A \cdot B \cdot \overline{C} + A \cdot \overline{C} \cdot D + \overline{A} \cdot C \cdot \overline{D} \]

\[ Y = \text{__________________________} \text{ MSOP} \]
4. Create a circuit for the following equation using only 3 Input AND gates and Inverters. (10 pt.)

\[ Y = (A \cdot B \cdot C \cdot \overline{B} \cdot C + D) ; \] Y.L, A.H, B.L, C.H, D.L \hspace{1cm} \textbf{Do Not Simplify the Equation!}

5. Derive the logic equation for the following circuit below. Show all \textit{intermediate terms as high true signals} for full credit. \textbf{DO NOT SIMPLIFY.} (9 pt.)

\[ Z.H = \text{______________________________} \]
6. For the circuit shown below, derive the logic equation for Z.L. **Do not simplify** your answer. (8 pt.)

For the circuit shown below, derive the logic equation for Z.L. **Do not simplify** your answer. (8 pt.)

\[ Z.L = \text{_______________________________} \]

7. Implement the following equation below using only **Tri-State Buffers (with a Low True Enable)**, **Open Collector Inverters** and **10K Resistors**. The best solution will receive the most points. (8 pt.)

\[ Y = /A*B + C*/D ; \text{ A.H, B.H, C.H, D.H, Y.L} \]
8. Design a circuit that multiplies two 2 bit signed numbers and has a four bit signed result, i.e. compute M1:0 x N1:0 = P3:0 where M & N are two bit signed numbers and P3:0 is a four bit signed number. Derive the block diagram & truth table for the device & show circuit required for P3. Assume: Positive Logic. Best design = most pts. (18 pt.)

Device Block Diagram Below (2)  
Device Logic Truth Table Below (11)  

MSOP Logic Equation & Circuit for P3 Below (5)
9. Two Bit Unsigned Divider Design. Fill in the truth table below to create a device that divides a two bit unsigned number by a two bit unsigned number. Your answer should be five bits accuracy with an implied decimal point between the second and third most significant bits. i.e. $A1:0 \text{ divided by } B1:0 = C4:0$  
Helpful Hint: $2^{-3} = 0.125$ (12 pt.)

<table>
<thead>
<tr>
<th>A1</th>
<th>A0</th>
<th>B1</th>
<th>B0</th>
<th>C4</th>
<th>C3</th>
<th>C2</th>
<th>C1</th>
<th>C0</th>
</tr>
</thead>
</table>

; Where A1, B1 and C4 are Most Significant Bits.
; Use X where unknown or don’t care.
; Note: Your binary output may contain
; approximation error but should be as close as
; possible to the actual divide result.

10. Counter Design. For the state diagram below, show the functional block diagram and the circuit required to create the least significant bit of the counter (D0). Assume D Flip-flops are available. Best circuit = highest points! (8 pt.)

Functional blk diagram =>

Next state table & LSB D flip-flop
Input circuit below =>

\begin{itemize}
\item X=1
\item 1
\item X=0
\item 0
\item X=1
\item 2
\item X=1
\item 3
\end{itemize}