Given: \( Y = \overline{AB} + C \) 

Logic Equation w/ A, L, B, H, C, H, Y, L

1. Write the Logic Truth Table?

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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<td>0</td>
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</table>

2. Write the Voltage Table?

<table>
<thead>
<tr>
<th>A. L</th>
<th>B. H</th>
<th>C. H</th>
<th>Y. L</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>L</td>
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<td>H</td>
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<td>H</td>
</tr>
</tbody>
</table>
3) Implement the Circuit using NAND gates only?

3a) Positive Logic Method

I. Draw the Logic Equation using ANDs & OR Gates.

II. Add inverters for complements in the Logic Equation.

III. Add inverters for lowtrue input and output signals.

IV. Simplify using existing hardware.

I. 

\[ y = \overline{AB} + C \]

II. 

\[ \begin{array}{c}
A \\
B \\
C
\end{array} \rightarrow \begin{array}{c}
D \\
y
\end{array} \]

III. \[ A_1, B, H, C, H, y_1 \]

IV. \[ \rightarrow = \rightarrow \rightarrow \]

\[ \begin{array}{c}
A \\
B \\
C
\end{array} \rightarrow \begin{array}{c}
D_1 \\
y
\end{array} \rightarrow \begin{array}{c}
D_2 \\
y
\end{array} \]

IV. Nands Only
3. Mixed Logic Method

I. Draw with selected gate in "AND" or "OR" configuration as needed.

i.e., selected gate = NAND

```
  D  →  D  AND configuration
```

```
  D  →  ⨁  OR Configuration
```

III. Look for mismatches in the circuit. Mismatches should correspond to complements in the logic equation.

IV. Add inverters to remove or add mismatches such that the existing mismatches all correspond to complements in the logic equation.

List of Mismatches

(a) active low input signal connected to active high input wire
(b) active high input signal connected to active low (bubble) wire
(c) active high output wire connected to an active low output signal
(d) active low output wire connected to an active high output signal
Mixed Logic Method (Continued)

I. \( Y = \overline{AB+C} \)

\[ \text{"AND" version of NAND} \rightarrow \text{"OR" version of NAND} \]

II. Look for mismatches

\[ \text{mismatch } \#1 \]
\[ \text{mismatch } \#2 \]
\[ \text{mismatch } \#3 \]

- We only want mismatches for \( \overline{AB+C} \)
- Mismatch \#1 & \#2 are not desired and should be removed with inverters
- Mismatch \#3 is \( \overline{AB+C} \) so this is okay
- Also need to create mismatch
III. Fixing Bad Mismatches & Creating one needed mismatch

- above circuit is complete but you should show:

\[
\overrightarrow{a} = \overrightarrow{b} = \overrightarrow{c}
\]

\[
\overrightarrow{d} = \overrightarrow{e}
\]
Extra Practice: Draw the circuit for \( Y = \overline{ABC} + D \)

Using \( \overline{NOR} \) w/ y.L, A.H, B.H, C.H, D.L signal definition

Positive Logic Method

I. \( \overline{A} \quad \overline{B} \quad \overline{C} \quad \overline{D} \rightarrow \overline{y} \)
II. \( \overline{A} \quad \overline{B} \quad \overline{C} \quad \overline{D} \rightarrow \overline{y} \)
III. \( y.L, D.L \)

Final Circuit

Mixed Logic

"Or" style "And" style

I. \( \overline{D} \rightarrow y \)
II. \( \overline{A} \rightarrow y \)
III. \( \overline{B} \rightarrow y \)
IV. \( \overline{C} \rightarrow y \)
V. \( \overline{D} \rightarrow y \)

where \( \overline{D} = \overline{y.L} \)

*1, 2, 4, 5 are mismatches!

*1 = bad, must remove  *4 = bad, remove
*2 = bad, must remove  *5 = bad, remove
*3 = okay, \( \overline{B} \) also, add mismatch

For \( \overline{A}.B.C \)

Final Circuit

I. \( A \rightarrow \overline{D} \rightarrow \overline{y.L} \)
II. \( B \rightarrow \overline{D} \rightarrow \overline{y.L} \)
III. \( C \rightarrow \overline{D} \rightarrow \overline{y.L} \)
IV. \( D \rightarrow \overline{D} \rightarrow \overline{y.L} \)

where \( \overline{D} = \overline{D} \)