Additional Problems:

1. Design a two bit unsigned multiplier. Show the logic table, K-Maps, MPOS & MSOP and then assume positive logic signal definitions to create a circuit using any gate. Choose the MPOS or MSOP version to minimize the gate design.

2. Given a 74HC138 and any other gates required (ANDs, ORs, Inverters), implement the following logic equations:

   \[ Y = A^*/B*C*D^*/E \quad ; \quad \text{assume all signals are low true} \]
   \[ Z = (A*B + C)(D^*/E) \quad ; \quad \text{assume inputs are low true and the output is high true} \]

3. Use a 4:1 Mux (with no global enable) and a minimum of other gates (ANDS, ORs & Inverters) to implement the following logic equation: \( F = A^*/B^*/C*D + B*C + /B*C*(E+/G) \); assume F.L, B.H, C.L, D.H, E.L, G.L

4. Find the logic equations for Y.L and Z.H below.

5. Design a single bit magnitude comparator block with high true inputs A, B, A>B, A<B, A=B and high true outputs A>B, A<B and A=B. Create a logic truth table, MSOP and implement with ANDs, ORs & Inverters.

6. Use the above block to create a 4 bit magnitude comparator.
Homework 4

Due: Friday, February 6th, 4 pm - usual drop-off location

7. Create a 4:1 multiplexer with high true inputs and outputs. Realize with NAND gates only.

8. Repeat the above (4:1 multiplexer) using inverters and tri-state devices only.

9. Add a high true global enable to the 4:1 multiplexer in #10.

10. Create a 16:1 multiplexer using the basic 4:1 multiplex block designed in #10.

11. Create an 8:3 Priority Encoder based on the Logic Truth Table below. Find the logic equations by inspection and implement with any gates available. Encoder Specifics: Inputs: I7:0, Outputs: C2:0, assume all signals are high true.

<table>
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<tr>
<th>I7 I6 I5 I4 I3 I2 I1 I0</th>
<th>C2 C1 C0</th>
</tr>
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<td>1 1 1</td>
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