1. Directly synthesize a circuit for the following equation using only 2 Input NOR gates only. (9 pt.)

\[ Y = A^* (B^*C) + E + D \]

; A.L, B.H, C.L, D.H, E.L, Y.H  \underline{Do Not Simplify the Equation!}

\[ \underline{Key} \]

\[ \sim \neg = \text{NOR} \]

\[ \neg \neg = \equiv \]

\[ \text{B.H} \rightarrow \text{A.L} \]

\[ \text{C.L}\rightarrow \text{D.H} \]

\[ \underline{Each \ gate = 1 \ pt.} \]

\[ \underline{Most \ optimal \ solution = Full \ credit} \]

\[ \underline{Any \ # \ of \ gates \ over \ 9 \ AND \ \underline{Correct}} \]

\[ \underline{\sim \ pt \ per \ \underline{-0.5 \ gate}} \]

\[ \underline{No \ key \ -2 \ pt} \]

\[ \underline{Incomplete \ key \ -0.5} \]

\[ \underline{Incorrect \ circuit \ or \ using \ simplified} \]

\[ \underline{\sim \sim \sim \sim \ \underline{9 \ pts \ depending}} \]

\[ \underline{Pg. \ Score =} \]
2. Find the **minimum sum of products** and **minimum product of sums** for the logic equation below using a K-Map. (14 pt.)

\[ Y = (A+B+C+D)/(A+/B+C+D)/(A+C+D)(B+/C+D)(A+/B+/D) \]

\[
\begin{align*}
Y (\text{MSOP}) &= \frac{\overline{A}B\overline{D} + \overline{B}D + A\overline{D} + \overline{A}C\overline{D}}{2} \\
Y (\text{MPOS}) &= \frac{(B+D)(A+B+\overline{D})(\overline{A}+C+D)}{2}
\end{align*}
\]

3. Derive the logic equations for the following signals listed after the circuit below. **Show all intermediate signals as HIGH true for partial credit purposes. DO NOT SIMPLIFY YOUR ANSWER!**

\[
\begin{align*}
\text{W.H} &= (A+B)(\overline{C}\overline{D}) \\
\text{Y.L} &= (A+B)(\overline{C}\overline{D}) + \overline{E}+\overline{G}
\end{align*}
\]
4. Simplify the equation below with De Morgan's Rule and Boolean Identities to find the MSOP. (10 pt.)


\[ \bar{X}Y\bar{Z} + \bar{X}Y\bar{W} + \bar{X}Z\bar{W} + \bar{X}Z\bar{W} + \bar{X}Y\bar{Z} \]

\[ Y = \bar{X}Z + \bar{Y}Z + XYW \]

5. A student would like to design a multiplier that computes the product of a 2 bit unsigned number times a 3 bit unsigned number. i.e. \( P = M1:0 \times N2:0 \) ; where all numbers are unsigned binary

How many bits are required for \( P \)? \( 5 \) (2 pt.)

Write the Canonical Sum of Products (CSOP) for the most significant bit of \( P \) based on inputs \( M1:0 \) and \( N2:0 \) below. (8 pt.)

- \( 3 \times 7 = 21 \)
- \( 3 \times 6 = 18 \)
- \( 3 \times 5 = 15 \)

\[ P4 = M1M0N2N1N0 + M1M0 \bar{N}2N1\bar{N}0 \]

-4 if 1 term is correct

\[ P4 = M1M0N2N1 -1 \text{ simplified} \]

Page 3
6 - 8. Perform the following addition, subtraction and multiplication. (9 pt.)

\[
\begin{array}{c}
10111 \\
111001 \\
101101 \\
+111111 \\
\hline
10100101
\end{array}
\]

3 [Wrong carry] 3

\[
\begin{array}{c}
0110112 \\
00010001 \\
-0111110 \\
\hline
0001001
\end{array}
\]

10101.01
\[
\begin{array}{c}
10101.01 \\
10101.00 \\
101.0101 \\
\hline
101111.1001
\end{array}
\]

9. For the circuit below, derive the logic equation for Z.H. Do not Simplify! (8 pt.)

\[
\text{Z.H} = \overline{E}G + \overline{E} \overline{G} + \overline{C} \overline{D} A \overline{B} \overline{E} \overline{G} + \overline{C} \overline{D} A \overline{B} \overline{E} \overline{G}
\]
10. Given the circuit below complete the voltage timing diagram for signals X and Y. Assume all devices have a 10nsec propagation delay. (8 pt.) Assume A=L, B=L, C=H initially.

Gate Propagation Delay is 10nsec!

11. For the circuit below derive the logic equation for Y and add the required missing Pull-up or Pull-down resistor to make Y a function of A,B,C,D, E, G and N. (10 pt.)

\[ Y.L = \left( A + \bar{B} \right) \left( C \bar{D} \right) \left( \overline{E} \right) \left( G \right) \left( \overline{N} \right) \]
12. Create a device that decrements a \textbf{4 bit Signed Number} by 1. \textbf{N3:0} is the \textbf{signed input} and \textbf{M3:0} is the \textbf{signed output} equivalent to \textbf{N3:0} – 1. For example, if a “3” is input to the device, the output should be “2”. One additional output, \( V \), should also be generated that indicates when an overflow occurs. For example, if decrementing an input by 1 creates an overflow condition, output \( V = 1 \), otherwise \( V = 0 \).

Draw the truth table for the device below:

<table>
<thead>
<tr>
<th>N3</th>
<th>N2</th>
<th>N1</th>
<th>N0</th>
<th>M3</th>
<th>M2</th>
<th>M1</th>
<th>M0</th>
<th>V</th>
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<td>0</td>
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</tr>
</tbody>
</table>

Derive the MSOP Logic Equation for \textbf{M0} and \textbf{V} (5 pt.):

\[
M_0 = \overline{N_0}
\]

\[
V = N_3 \overline{N_2} \overline{N_1} \overline{N_0}
\]