Open book and open notes, 90-minute examination. No electronic devices are permitted.

Page 1) 9 points ________________ Page 2) 23 points ________________

Page 3) 18 points ________________ Page 4) 17 points ________________

Page 5) 18 points ________________ Page 6) 15 points ________________

TOTAL ________________ of 100

Re-grade requests must be handed in the day exams are returned in class. Write the problem number you wish reviewed. A maximum of three review problems is allowed. Do not write anywhere else on the exam other than below or you will receive a zero on the exam.

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1. Directly synthesize a circuit for the following equation using only 2 Input NOR gates only. (9 pt.)

   \[ Y = \overline{A} \cdot \overline{(B \cdot C)} + E + D \; ; \; A.L, B.H, C.L, D.H, E.L, Y.H \]  Do Not Simplify the Equation!
2. Find the **minimum sum of products** and **minimum product of sums** for the logic equation below using a K-Map. (14 pt.)

\[ Y = \overline{(A+B+C+D)}(\overline{A}+B+C+D)(\overline{A}+C+D)(B+\overline{C}+D)(A+B+D) \]

\[ Y (MSOP) = \text{________________________________________} \quad (8) \]

\[ Y (MPOS) = \text{________________________________________} \quad (6) \]

3. Derive the logic equations for the following signals listed after the circuit below. *Show all intermediate signals as HIGH true for partial credit purposes. DO NOT SIMPLIFY YOUR ANSWER!*

\[ W.H = \text{________________________________________} \quad (5 \text{ pt.}) \]

\[ Y.L = \text{________________________________________} \quad (4 \text{ pt.}) \]
4. Simplify the equation below with De Morgan’s Rule and Boolean Identities to find the MSOP. (10 pt.)


5. A student would like to design a multiplier that computes the product of a 2 bit unsigned number times a 3 bit unsigned number. i.e. \( P = M1:0 \times N2:0 \); where all numbers are unsigned binary

How many bits are required for \( P \)? (2 pt.)

Write the Canonical Sum of Products (CSOP) for the most significant bit of \( P \) based on inputs \( M1:0 \) and \( N2:0 \) below. (8 pt.)
6 – 8. Perform the following addition, subtraction and multiplication. (9 pt.)

\[
\begin{align*}
&\quad 111001 \\
&101101 \quad - \quad 01111110 \\
&+ \quad 111111 \\
&\quad 1010101
\end{align*}
\]

9. For the circuit below, derive the logic equation for Z.H. **Do not Simplify!** (8 pt.)

Z.H = ____________________________
10. Given the circuit below complete the voltage timing diagram for signals X and Y. Assume all devices have a 10nsec propagation delay. (8 pt.) **Assume A=L, B=L, C=H initially.**

11. For the circuit below derive the *logic equation for Y* and *add the required missing Pull-up or Pull-down resistor* to make Y a function of A,B,C,D, E, G and N. (10 pt.)

Y.L = ________________________________________________________________________________
12. Create a device that decrements a 4 bit Signed Number by 1. N3:0 is the signed input and M3:0 is the signed output equivalent to N3:0 – 1. For example, if a “3” is input to the device, the output should be “2”. One additional output, V, should also be generated that indicates when an overflow occurs. For example, if decrementing an input by 1 creates an overflow condition, output V = 1, otherwise V = 0.

Draw the truth table for the device below:

<table>
<thead>
<tr>
<th>N3</th>
<th>N2</th>
<th>N1</th>
<th>N0</th>
<th>M3</th>
<th>M2</th>
<th>M1</th>
<th>M0</th>
<th>V</th>
</tr>
</thead>
</table>

Derive the MSOP Logic Equation for M0 and V (5 pt.):