1. Perform the following binary additions and subtractions by hand. For full credit, show all your work below. Assume the numbers are all unsigned binary. (3,2,3 pt.)

\[
\begin{align*}
111111 & \quad 10101010 & \quad 1101.001 \\
101010 & - \quad 0111011 & \times \quad 100.110 \\
+ \quad 111111 & \\
\end{align*}
\]

2. Write -27 as a 16 bit Signed Hex number. (2 pt.)

3. When multiplying (2) 8 bit Signed numbers (A * B), how many bits are required in the final answer such that no overflow will ever occur? Hint: Solve for a smaller word length. (3 pt.)
4. Directly synthesize a circuit for the following Logic Equation using only 2 input NOR gates. (9 pt.)

\[ Y = \overline{A} + ((B+C) \cdot D) \quad ; \ A, B, C, D, Y.H \quad \text{Do Not Simplify the Equation!} \]

5. Show the ALL the CONNECTIONS below to implement the above circuit in the two 74HC02 NOR ICs below. (7 pts.)

9. Derive the logic equations for the following signals listed after the circuit below. Show all intermediate signals as HIGH true for partial credit purposes. DO NOT SIMPLIFY YOUR ANSWER!

\[ Y.H = \text{________________________} \quad (9 \text{ pt.}) \]
10. Find the **minimum sum of products** and **minimum product of sums** for the logic equation below using a K-Map.

\[(B+C+D)(\overline{A}+B+\overline{C}+D)(A+\overline{C}+D)(B+D)(A+B+\overline{C}+D)(\overline{A}+\overline{B}+\overline{D})\]

\[Y (MSOP) = \text{__________________________} \quad (5)\]

\[Y (MPOS) = \text{__________________________} \quad (5)\]

11. Given the circuit below complete the **voltage timing diagram** for signals X and Y. Assume all devices have a **10 nsec** propagation delay. (9 pt.) **Assume A = B = Y = L, C = W = H initially.**

![Circuit Diagram]

\[
\begin{align*}
\text{A} & \\
\text{B} & \\
\text{C} & \\
\text{W} & \\
\text{Y} & \\
\end{align*}
\]

\[
\begin{array}{cccccccc}
5 & 10 & 15 & 20 & 25 & 30 & 35 & 40 & 45 & 50 & 55 & 60 \\
\text{A} & \\
\text{B} & \\
\text{C} & \\
\text{W} & \\
\text{Y} & \\
\end{array}
\]

\[=> t_p 10 \text{ ns } <=\]
12. Simplify the equation below with **De Morgan’s Rule** and **Boolean Identities** to find the **MSOP**. (10 pt.)

\[
\]

\[
Y = \frac{\text{expression}}{\text{expression}} \quad \text{MSOP}
\]

13. Lucky #$%@##! 13! Perform the following **Unsigned Binary division** below by hand. **Show at least 6 fractional binary bits in your answer.** (5 pt.)

\[
\begin{array}{c}
11.01 \\
\hline
1011.101
\end{array}
\]
14. For the circuit below find the MSOP for W.H and Y.L. (10 pt.)

W.H = ______________________________________________________________________ MSOP (3 pt.)

Y.L = ______________________________________________________________________ MSOP (7 pt.)

15. Implement the logic equation \( Z = \overline{A}/\overline{B}/C \) (Z.L, A.L, B.H, C.L) in hardware using Open Collector Inverters and 1K ohm resistors. (6 pt.)
16A. Design a **Signed Multiplier** that **multiplies a 3 bit signed (2’s complement) number by -7**. The input is therefore a 3 bit signed number and output should be the input value multiplied by a constant (-7) Assume all inputs & outputs are high true. Create a Logic Truth Table below for the device below. (8 pt.)

16B. Determine the MSOP logic equation for the output Most Significant Bit (MSB). (4 pt.)